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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,857	12/22/2000	Richard P. Modelski	120-100	8573

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EXAMINER	
TRUONG, LAN DAI T	
ART UNIT	**PAPER NUMBER**
2152	
MAIL DATE	**DELIVERY MODE**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/741,857	MODELSKI ET AL.	
	Examiner	Art Unit	
	Lan-Dai Thi Truong	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2000* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is response to communications: application, filed on 12/22/2000; amendment filed 02/12/2007. Claims 1-18 are pending; claim 4 is cancelled; claims 1-3, 5, 17 are amended

2. The applicant's arguments filed on 09/05/2006 have fully considered but they are moot in view with new ground for rejections

Response to Arguments

3. In response to applicant's arguments that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., multi-IP packet) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

4. In response to applicant's argument that there is no suggestion to combine the Epps into the Davis, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir.

1992). In this case, both of the Davis and the Epps teach the same environment i.e. pipelined processing, see (Davis: column 2, lines 1-20, lines 35-67; Epps: column 5, lines 1-67; column 6, lines 1-25)

5. In response to applicant's argument that there is no suggestion to combine the Eickemeyer into the Davis-Epps, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, all of the Davis, the Epps and the Eickemeyer teach the same environment i.e. pipelined processing, see (Davis: column 2, lines 1-20, lines 35-67; Epps: column 5, lines 1-67; column 6, lines 1-25; Eickemeyer: column 4, lines 51-67)

Claim rejections-35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or descried as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5, 17 are rejected under 35 U.S.C 103(a) as being un-patentable over Davis et al. (U.S. 5,357,617) in view of Epps et al. (U.S. 6,813,243)

Regarding claim 1:

Davis discloses the invention substantially as claimed, including a method, which can be implemented in a computer hardware or software code for processing a plurality of independent multi-packet threads, comprising:

Retrieving a first packet from a first packet thread: (Davis discloses a pipelined processor for substantially concurrent processing of a plurality of program instructions threads; in Davis's system, "an instruction in a first thread" which shares functionality with "a first packet from a first packet thread" is fetched for operating by the pipelined processor: column 2, lines 1-20, lines 35-67)

Retrieving a second packet from a second packet thread: (in Davis's system, "an instruction in a second thread" which shares functionality with "a second packet from a second packet thread" is fetched for operating via the pipelined processor: column 2, lines 1-20, lines 35-67)

Processing the first packet in a first stage of processing pipeline; and forwarding the first packet to a next stage of the processing while forwarding the second packet into the first stage of the processing pipeline such that the first and the second packets can be processed simultaneously in the processing pipeline; and wherein the independence of packet threads eliminates packet processing delays: (Davis discloses the pipelined processor processes steps of: "fetching" which shares functionality with "a first stage" as claimed the instruction from one of the instructions thread, then "decoding" which shares functionality with "a next stage" as claimed the fetched instruction; while simultaneously fetching another instruction from a

different one of the instructions threads; Davis also mentions his invention pipelined processor can be used for eliminating time delay purpose: column 2, lines 1-5, 10-20, lines 35-67)

However, Davis does not explicitly disclose IP packet

In analogous art, Epps discloses method for using pipelined switch/linecard for parallel operating on numbers of IP/ or TCP packets for transmitting them over IP/ or TCP communication network, see (column 5, lines 1-67; column 6, lines 1-25).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Davis's ideas of using the pipelined processor for substantially concurrent processing of a plurality of program instructions threads simultaneously into Epps's pipelined switch/linecard which parallel operates on numbers of IP packets for transmitting them over IP/ or TCP communication network in order to be able to employ a well-know standard into Epps's system for saving resources and development time to bring up at least one advantage i.e. provide more flexibilities for IP network switch system, see (Epps: column 2, lines 7-65; column 8, lines 1-8)

Regarding claim 5:

This claim is rejected under rationale of claim 1

Regarding to claim 17:

In addition to rejection in claim 5, Davis-Epps further discloses a thread identifier identifying a subset registers allocated to corresponding independent multi-packet threads, the subset of registers selected from among a set of registers, and wherein the subsets associated with each one of the plurality of independent multi-packet threads are unique: (Davis discloses

multiple independent instruction threads register to multiple-threads processor: abstract, lines 4-9; column 5, lines 32-67; column 6, lines 1-60)

Regarding to claim 2:

In addition to rejection in claim 1, Davis-Epps further discloses transferring packet from an input buffer to a packet task manager; dispatching the packet from the packet task manager to an analysis machine; classifying the packet in the analysis machine; and modifying and forwarding the packet in a packet manipulator: (Epps teaches methods for transferring data from an input buffer (Fig 2, item 215) to a packet task manager (Fig 2, item 130, Col. 5, lines 50-55); dispatching the data from the packet task manager to an analysis machine (Fig 2, data travel from item 215 to 220; Col. 6, lines 33-37); classifying the data in the analysis machine (Col. 6, lines 33-37); and modifying and forwarding the data in a packet manipulator (Fig 4, item 450 and 460; Col. 6, lines); a packet manipulator (Epps, Fig 4, item 450, 460) operationally connected to said analysis machine (Epps, Fig 4, data travel from 220 to item 450 and 460).

Regarding to claim 3:

In addition to rejection in claim 1, Davis-Epps further discloses forwarding data to output after modifying: (Epps teaches forwarding packet to output after modifying: Fig. 2, item 1430; Col. 42, lines 10-21)

Claims 6-16 and 18 are rejected under 35 U.S.C 103(a) as being un-patentable over Davis-Epps in view of Eickemeyer (U.S. 6,694,425)

Regarding claim 6:

In addition to rejection in claim 1, Davis-Epps further discloses pipeline is dedicated to directly manipulating individual data bits of a bit field (Epps, Col. 6, lines 50-67; Col. 14, lines

1-3); a packet task manager (Epps, Fig 2, item 130, Col. 5, lines 50-55) operationally connected to said analysis machine (Epps, Fig 2, data travel from item 215 to 220; Col. 6, lines 33-37); a packet manipulator (Epps, Fig 4, item 450, 460) operationally connected to said analysis machine (Epps, Fig 4, data travel from 220 to item 450 and 460).

However, Davis- Epps does not explicitly disclose a machine having multiple pipelines

In analogous art, Eickemeyer discloses the decode unit may have multiple pipelines: (column 9, lines 19-24)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Eickemeyer's ideas of including multiple pipelines into Davis-Epps's system in order to be able to employ well-know resources/standard into the Davis-Epps's system for saving development time and to provide at least one advantage such as faster responding, and reducing delay time/ and memory utilization, see (Eickemeyer: column 4, lines 4-48; column 9, lines 18-41)

Regarding claim 7:

This claim is rejected under rationale of claim 6

Regarding claim 8:

In addition to rejection in claim 1, Davis-Epps- Eickemeyer further discloses 32 threads, although Davis-Epps- Eickemeyer does not specifically disclose analysis machine has 32 threads, such limitations are merely a matter of design choice and would have been obvious in system of Davis-Epps- Eickemeyer

Regarding claim 9:

In addition to rejection in claim 6, Davis-Epps- Eickemeyer further discloses a packet task manager (Epps, Fig 2, item 130, Col. 5, lines 50-55) operationally connected to said analysis machine (Epps, Fig 2, data travel from item 215 to 220; Col. 6, lines 33-37); a packet manipulator (Epps, Fig 4, item 450, 460) operationally connected to said analysis machine (Epps, Fig 4, data travel from 220 to item 450 and 460); a global access bus including a master request bus (Epps, Fig 4, item 496) and a slave request bus (Epps, Fig 4, item 497) separated from each other and pipelined (Epps, Fig 4, items 410-460

Regarding claim 10:

In addition to rejection in claim 6, Davis-Epps- Eickemeyer further discloses an external memory engine (Fig 4, item 215, external FIFO externally connected to analysis machine) operationally connected to said analysis machine (Epps, Fig 4, item 420, Col. 6, lines 30-35, wherein the analysis machine classifies packet data); a hash engine (Epps, Fig. 4, item 430; Col. 24, lines 24-28) operationally connected to said analysis machine (Epps, Col. 24, lines 24-28)

Regarding claims 11-12:

In addition to rejection in claim 9, Davis-Epps- Eickemeyer further discloses packet input global access bus program code (Epps: Col. 11, lines 55-60, wherein the instructions are the software code, Fig 6, item 610, 630) used for flow of data packet information from a flexible input data buffer (Epps, Fig 6, item 480) to an analysis machine (Epps, Fig 6, item 420; Col. 11, lines 55-60; Col. 6, lines 23-37, the packet header information is retrieved and processed by the pre-process stage)

Regarding claim 13:

In addition to rejection in claim 9, Davis-Epps- Eickemeyer further discloses statistics data global access bus software code (Epps: instructions residing in pipeline control Fig 4, item 495; Col. 11, lines 55-65, wherein instructions originated from pipeline control 495 dictates the-execution of the stages note, that the packet data is passed to the next stage upon completion of the current stage of execution, therefore, pipeline control is used for communications purposes between analysis machine and the packet manipulator) used for connection of an analysis machine (Fig 4, item 420) to a packet manipulator (Epps, Fig 4, item 460)

Regarding claim 14:

In addition to rejection in claim 9, Davis-Epps- Eickemeyer further discloses private data global access bus software code (Epps discloses instructions residing in pipeline control Fig 4, item 495; Col. 11, lines 55-65, wherein instructions originated from pipeline control 495 dictates the execution of the stages note, that the packet data is passed to the next stage upon completion of the current stage of execution, therefore, pipeline control is used for communications purposes between analysis machine and the internal memory engine) for connection of an analysis machine (Fig 4, item 420) to an internal memory engine sub-module (Epps, Fig 4, item 480, Col. 11, lines 55-65, wherein the instruction fetches allows for connection between the PreP stage / analysis machine and the packet header buffer/ internal memory engine sub-module, look up is done through pipeline control Fig 4, item 495)

Regarding claim 15:

In addition to rejection in claim 9, Davis-Epps- Eickemeyer further discloses lookup global access bus software code (Epps discloses instructions residing in pipeline control Fig 4, item 495; Col. 11, lines 55-65, wherein instructions originated from pipeline control 495 dictates

the execution of the stages note, that the packet data is passed to the next stage upon completion of the current stage of execution, therefore, pipeline control is used for communications purposes between analysis machine and the internal memory engine) used for connection of an analysis machine (Fig 4, item 420) to an internal memory engine sub-module (Epps, Fig 4, item 480, Col. 11, lines 55-65, wherein the instruction fetches allows for connection between the PreP stage / analysis machine and the packet header buffer/ internal memory engine sub-module, look up is done through pipeline control Fig 4, item 495)

Regarding claim 16:

In addition to rejection in claim 9, Davis-Epps- Eickemeyer further discloses results global access bus software code (Epps, Col. 10, lines 5-10, the value of n is a programmable value, indicating amount of data to send to fetch stage, Fig 5, item 410) used for providing flexible access to an external memory (Epps, Col. 10, lines 5-10, amount of data received can be adjusted)

Regarding claim 18:

In addition to rejection in claim 9, Davis-Epps- Eickemeyer further discloses a bi-directional access port operationally connected to said analysis machine (Epps, Col. 25, lines 1-7, wherein the input/output port are PPP/HDLC); an input buffer (Epps, Fig 2, item 215) operationally connected to said analysis machine (input buffer operationally connected to Prep Stage Fig 4, item 420 / analysis machine through the pipeline); and an output buffer (Epps, Fig 2, item 1430) operationally connected to said analysis machine (transmit FIFO operationally connected to Prep Stage Fig. 4, item 420 through the switch fabric)

The prior arts made of records and not relied upon are considered pertinent to applicant's disclosure. The following patents and publications are cited to further show the state of the art with respect to "Multi-thread packet processor": 6889319; 20020002667; 7096343; 2002/0062435; 6477562; 6920635; 6535878; 6181990; 7093109; 6952824; 5764912; 6976095; 6768716

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusions

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan-Dai Thi Truong whose telephone number is 571-272-7959. The examiner can normally be reached on Monday- Friday from 8:30am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob A. Jaroenchonwanit can be reached on 571-272-3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

04/28/2007

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SUPERVISORY PATENT EXAMINER
4/30/07